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EXAMINER	
TRAN, TAN N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,704	AHN ET AL.	
	Examiner	Art Unit	
	TAN N TRAN	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 04/08/04*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-51,55-71,73-80,82-116,118,120-126 and 128-142* is/are pending in the application.

4a) Of the above claim(s) *30-49* is/are withdrawn from consideration.

5)☒ Claim(s) *22 and 137-142* is/are allowed.

6)☒ Claim(s) *20,21,23-29,50,51,55-71,73-80,82-116,118,120-124,126 and 128-136* is/are rejected.

7)☒ Claim(s) *125* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 55-57,59,62-64 stand rejected under 35 U.S.C. 102(b) as being anticipated by Casto (5,014,113).

With regard to claim 55, Casto et al. discloses a lead frame comprising a die pad 40, a plurality of leads 28 disposed around the die pad 40 and a tie bars 46 connected to and disposed around the die pad 40, wherein the die pad 40 comprises a chip attaching part and a peripheral part surrounding the chip attaching part; a semiconductor chip 12 mounted to the die pad chip attaching part, the chip 12 having a plurality of electrode pads 14, wherein the plurality of electrode pads 14 are electrically interconnected to the leads 28, and wherein each of leads 28 comprises integrally connected inner leads and outer leads; an encapsulant encapsulating the semiconductor chip 12 to form a package body 36, wherein the inner leads are encapsulated by the encapsulant and the outer leads are external to the encapsulant; and the chip attaching part having a first thickness and the inner leads 28 totally having a constant second thickness greater

than the first thickness wherein the chip attaching part and the peripheral part have the same thickness. (Note figs.1, 2 of Casto).

With regard to claim 56, Casto discloses the inner leads of the leads 28 are formed of a single layer. (Note figs.1, 2 of Casto).

With regard to claim 57, Casto discloses the first thickness is between about 30 percent to 50 percent of the second thickness. (Note lines 20-24, column 5, figs.1,2 of Casto et al.).

With regard to claim 59, Casto discloses the die pad 40 is located below the leads 28. (Note fig.1 of Casto et al.).

With regard to claim 62, Casto discloses upper and lower portions of the package body with reference to the leads (18,28) have different thickness each other. (Note fig.1 of Casto).

With regard to claim 63, Casto discloses the tie bar 46 has the same thickness as the leads 18. (Note figs.1,2 of Casto).

With regard to claim 64, Casto discloses the tie bar 46 has the same thickness as the die pad peripheral part. (Note figs.1,2 of Casto).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 20-24,28,58,71,73-80,86-96,100,102-110,114,116,133-134,136 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Nokita (JP-2000-124396) in view of Casto (5,014,113).

With regard to claims 20,21,58,71,74,75,87,88,102,116,133,134, Nokita discloses a semiconductor package device having 0.5mm or less of thickness comprising: a lead frame comprising a die pad 1, a plurality of leads 2 disposed around the die pad 1 wherein the die pad 1 comprises a chip attaching part having a first thickness and disposed below the leads 2; a peripheral part surrounding and protruding away the chip attaching part; first and second semiconductor chips (5A,5B) mounted to the die pad chip attaching part, wherein the first semiconductor chip 5A is bonded to a top surface of the chip attaching part and the second semiconductor chip 5B is bonded to a bottom surface of the chip attaching part; a package body 8 encapsulating the semiconductor chips (5A,5B); and bonding wires 7 configured to electrically connect the semiconductor chips (5A,5B) and leads 2, leads 2 having the inner leads are encapsulated by the package body 8 and the outer leads are exposed from the package body 8; wherein the inner leads having a second thickness, wherein the first thickness is smaller than the second thickness, wherein the peripheral part have a thickness equal to the second thickness of the inner leads, and wherein the peripheral part 1B protrudes toward the second semiconductor chip 5B and away from the first semiconductor chip 5B or the peripheral part 1A protruding towards the first semiconductor chip 5A and away from the second semiconductor chip 5B, wherein the bonding wires 7A connected to one of the semiconductor chips 5A are shorter than the bonding wires 7B connected to the other semiconductor chip 5B. (Note see attachment #1, fig.1 of Nokita).

Nokita does not disclose the first and second semiconductor chips each having a plurality of electrode pads and a tie bar connected to the die pad.

However, Casto discloses the chip 12 having a plurality of electrode pads 14, wherein the plurality of electrode pads 14 are electrically interconnected to the leads 28, a tie bars 46 connected to and disposed around the die pad 40. (Note figs.1, 2 of Casto).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Nokita's device having the first and second semiconductor chips each having a plurality of electrode pads and a tie bar connected to the die pad such as taught by Casto in order to secure an electrical connection between the semiconductor chips 5 and leads 2, and secure the interface between semiconductor chips and the die pads.

With regard to claims 23,76,91,105, Nokita and Casto do not disclose bonding wires are connected by balls formed on the surface of the leads and stiches formed on the electrode pads. However, it would have been obvious to one of ordinary skill in the art to form bonding wires are connected by balls formed on the surface of the leads and stiches formed on the electrode pads in order to secure the electrical connection between semiconductor chips and the leads.

With regard to claims 24,77,92,106, Nokita and Casto do not disclose metal bumps are formed on the electrode pads of the chip and wherein the stiches are formed on the metal bumps. However, it would have been obvious to one of ordinary skill in the art to form metal bumps are formed on the electrode pads of the chip and wherein the stiches are formed on the metal bumps in order to secure the interface between semiconductor chips and the die pads.

With regard to claim 28, Nokita and Casto disclose all the claimed subject matter except for a thickness of the package body is about 580 micrometer, a thickness of the die pad

peripheral part is about 100 micrometer, and a thickness of the chip attaching part is about 40 micrometer. However, it would have been obvious to one of ordinary skill in the art to form for a thickness of the package body is about 580 micrometer, a thickness of the die pad peripheral part is about 100 micrometer, and a thickness of the chip attaching part is about 40 micrometer in order to simplify the structure and fabrication to reduce the assembly cost of the device and to reduce the thickness or height of the device, because such structure is conventional in the art for forming a compact multi-chip package.

With regard to claims 86,100,114, Nokita and Casto disclose all the claimed subject matter except for the electronic apparatus is a memory card. However, it would have been obvious to one of ordinary skill in the art to form the electronic apparatus is a memory card, because such structure is conventional in the art for forming a compact multi-chip package.

With regard to claims 89,103, Nokita discloses the inner leads of the leads 2 are formed of a single layer. (Note fig.1 of Nokita).

With regard to claims 73,90,104, Nokita discloses the first thickness is between about 30% to 50% of the second thickness. (Note fig.1 of Nokita).

With regard to claims 79,80,94,95,108,109, Nokita and Casto do not disclose the tie bar has the same thickness as the leads wherein the tie bar has the same thickness as the die pad peripheral part. However, it would have been obvious to one of ordinary skill in the art to form disclose the tie bar has the same thickness as the leads wherein the tie bar has the same thickness as the die pad peripheral part in order to secure the interface between semiconductor chips and the die pads.

With regard to claims 96,110, Nokita discloses the peripheral part of the die pad 1 protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the thickness of the leads 2. (Note fig.1 of Nokita).

With regard to claims 78,93,107, Nokita and Casto do not disclose an upper portion of the package body above the leads and a lower portion of the package body below the leads have different thicknesses. However, it would have been obvious to one of ordinary skill in the art to form an upper portion of the package body above the leads and a lower portion of the package body below the leads have different thicknesses because such structure is conventional in the art for forming a compact multi-chip package.

With regard to claim 136, Nokita discloses the peripheral part protrudes upward from the chip attaching part. (Note fig.1 of Nokita).

Claim 135 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nokita (JP-2000-124396) in view of Casto (5,014,113) and further in view of Kouda (5,818,105).

With regard to claims 135, Nokita and Casto do not disclose the peripheral part protrudes from only one side of the chip attaching part.

However, Kouda discloses the peripheral part protrudes from only one side of the chip attaching part. (Note fig. 8 of Kouda).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Nokita and Casto's device having the peripheral part protrudes from only one side of the chip

attaching part such as taught by Kouda in order to secure the semiconductor chip on the die pad of the lead frame.

Claims 25-27,29,82-84,97-99,111-113 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Nokita (JP-2000-124396) in view of Casto (5,014,113) and further in view of Huang (2002/0113305).

With regard to claims 25,82,83,97,98,111,112, Nokita and Casto do not disclose the die pad comprises divided first and second die pads wherein the first and second die pads each include a chip attaching part and peripheral part.

However, Huang discloses the die pad comprises divided first and second die pads (410,440) wherein the first and second die pads (410,440) each include a chip attaching part and peripheral part. (Note fig. 1 of Huang).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Nokita and Casto's device having the die pad comprises divided first and second die pads wherein the first and second die pads each include a chip attaching part and peripheral part such as taught by Huang in order to provide more space for accommodating semiconductor chips.

With regard to claim 26, Huang discloses the first and second die pads (410,440) each include a chip attaching part and a peripheral part. (Note fig. 1 of Huang).

With regard to claims 27,29,84,99,113, Nokita and Casto do not disclose an adhesive bonds the semiconductor chip to the die pad chip attaching part, and an adhesive is attached to

the backside of the chip in a wafer state to bond the semiconductor chips to the chip attaching part.

However, Huang discloses an adhesive 11a bonds the semiconductor chip to the die pad chip attaching part. An adhesive 11b is attached to the backside of the chip in a wafer state to bond the semiconductor chips (12a,12b) to the chip attaching part. (Note fig. 6 of Huang).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Nokita and Casto et al.'s device having an adhesive bonds the semiconductor chip to the die pad chip attaching part, and an adhesive is attached to the backside of the chip in a wafer state to bond the semiconductor chips to the chip attaching part such as taught by Huang in order to secure the interface between semiconductor chips and the die pads.

Claims 60,70 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Casto (5,014,113).

With regard to claim 60, Casto et al. discloses the plurality of electrode pads 14 are electrically interconnected to the leads 28 via bonding wires 34.

Casto et al. does not disclose bonding wires are connected by balls formed on the surface of the leads and stiches formed on the electrode pads. However, it would have been obvious to one of ordinary skill in the art to form bonding wires are connected by balls formed on the surface of the leads and stiches formed on the electrode pads in order to secure the interface between semiconductor chips and the die pads.

With regard to claim 61, Casto discloses metal bumps are formed on the electrode pads 14 of the chip 12. (Note lines 1-7, column 4, fig. 1 of Casto).

Casto does not disclose the stiches are formed on the metal bumps. However, it would have been obvious to one of ordinary skill in the art to form the stiches are formed on the metal bumps in order to secure the interface between semiconductor chips and the die pads. (Note lines 1-7, column 4, fig. 1 of Casto).

With regard to claim 70, Casto does not disclose the semiconductor chip is a memory device and wherein the adhesive is a film made of an epoxy resin. However, it would have been obvious to one of ordinary skill in the art to form the semiconductor chip is a memory device and wherein the adhesive is a film made of an epoxy resin in order to secure the semiconductor chip on the die pad of the lead frame and because such structure is conventional in the art for forming a compact multi-chip package.

Claims 65 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Casto (5,014,113) in view of Nokita (JP-2000-124396).

With regard to claim 65, Casto does not disclose the peripheral part protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the thickness of the leads.

However, Nokita discloses the peripheral part of the die pad 1 protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the thickness of the leads 2. (Note fig.1 of Nokita).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Casto's device having the peripheral part protrudes in both vertical directions from the chip attaching

part, and the thickness of the peripheral part is equal to the thickness of the leads such as taught by Nokita because such structure is conventional in the art for forming a compact multi-chip package.

Claims 66-68,133 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Casto (5,014,113) in view of Huang (2002/0113305).

With regard to claim 66, Casto does not disclose the die pad comprises divided first and second die pads.

However, Huang discloses the die pad comprises divided first and second die pads (410,440). (Note fig. 1 of Huang).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Casto's device having the die pad comprises divided first and second die pads such as taught by Huang in order to secure semiconductor dies to be separated from the die pads of the leadframe.

With regard to claim 67, Huang discloses the first and second die pads (410,440) each include a chip attaching part and a peripheral part. (Note fig. 1 of Huang).

With regard to claim 68, Casto et al. does not disclose an adhesive bonds the semiconductor chip to the die pad chip attaching part.

However, Huang discloses an adhesive 11a bonds the semiconductor chip to the die pad chip attaching part. (Note fig. 6 of Huang).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Casto et al.'s device having an adhesive bonds the semiconductor chip to the die pad chip attaching part such as taught by Huang in order to secure the interface between semiconductor chips and the die pads.

With regard to claim 133, Huang discloses the semiconductor chip 12a and another semiconductor chip 12b are of the same type. (Note fig. 6 of Huang).

Claims 69,85,101,115 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Casto (5,014,113) in view of Kozono (6,177,718).

With regard to claims 69,85,101,115, Casto et al. does not disclose the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires.

However, Kozono discloses the lead frame 13 is made of iron-nickel alloy or copper alloy, and wherein the bonding wires 14 are gold wires. (Note lines 16-20, column 6, fig. 21 of Kozono).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Casto et al.'s device having the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires such as taught by Kozono in order to prevent the lead frame from broken.

Claims 50,51,120-124,126,132 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji et al. (4,855,807) in view of Nokita (JP-2000-124396) and further in view of Casto (5,014,113).

With regard to claim 50, Yamaji et al. discloses a semiconductor package device comprising: a lead frame 4 including a die pad 2, a plurality of single-layer leads 4 disposed around the die pad 2, and a tie bar 1 disposed around and connected to the die pad 2, wherein the die pad 2 includes a chip attaching part and a peripheral part surrounding the chip attaching part, the chip attaching part and the peripheral part having the same thickness, a semiconductor chip 3 connected to the chip attaching part; a package body 6 for encapsulating the semiconductor chip 3; bonding wires 5 configured to electrically connect the semiconductor chip to the leads 4, wherein each of the plurality of single-layer leads 4 comprises an inner lead bonded to the bonding wire 5 and encapsulated by the package body and an outer lead integral to the inner leads and extending from the package body; and wherein the chip attaching part has a first thickness and the inner lead has a second thickness that is greater than the first thickness. (Note figs. 1-3 of Yamaji et al.).

Yamaji et al. does not disclose the semiconductor package device having a package body of less than 0.7 mm of thickness.

However, Nokita discloses the semiconductor package device having a package body of less than 0.7 mm of thickness. (Note lines 1,2, paragraph 0014 of translation (of record), fig. 1 of Nokita).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Yamaji et al.'s device having the semiconductor package device having a package body of less than 0.7 mm of thickness such as taught by Nokita in order to obtain the storage capacity.

Yamaji et al. and Nokita disclose all the claimed subject matter except for a semiconductor chip having a plurality of electrode pads. Further, Casto discloses the semiconductor chip 12 having a plurality of electrode pads 14. (Note fig. 1 of Casto).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Yamaji et al. and Nokita's device having a semiconductor chip having a plurality of electrode pads such as taught by Casto in order to secure electrical connection between the semiconductor and lead frame.

With regard to claims 51,132, Yamaji et al., Nokita and Casto disclose all the claimed subject matter except for the electronic apparatus is a memory card. However, it would have been obvious to one of ordinary skill in the art to form the electronic apparatus is a memory card, because such structure is conventional in the art for forming a compact multi-chip package.

With regard to claim 120, Nokita discloses another semiconductor chip 5B attached to a back side of the chip attaching part. (Note see attachment #1 of Nokita).

With regard to claim 121, Yamaji et al. the die pad 2 is located below the leads 4. (Note fig. 3 of Yamaji et al.).

With regard to claim 122, Yamaji et al., Nokita and Casto disclose do not disclose bonding wires are connected by balls formed on the surface of the leads and stiches formed on the electrode pads. However, it would have been obvious to one of ordinary skill in the art to form bonding wires are connected by balls formed on the surface of the leads and stiches formed on the electrode pads in order to secure the electrical connection between semiconductor chips and the leads.

With regard to claim 123, Yamaji et al., Nokita and Casto disclose do not disclose metal bumps are formed on the electrode pads of the chip and wherein the stiches are formed on the metal bumps. However, it would have been obvious to one of ordinary skill in the art to form metal bumps are formed on the electrode pads of the chip and wherein the stiches are formed on the metal bumps in order to secure the interface between semiconductor chips and the die pads.

With regard to claim 124, Yamaji et al., Nokita and Casto disclose do not disclose an upper portion of the package body above the leads and a lower portion of the package body below the leads have different thickness. However, it would have been obvious to one of ordinary skill in the art to form an upper portion of the package body above the leads and a lower portion of the package body below the leads have different thickness because such structure is conventional in the art for forming a compact multi-chip package.

With regard to claim 126, Yamaji et al. the tie bar 1 has the same thickness as the die pad peripheral part of die pad 2. (Note figs. 1-3 of Yamaji et al.).

Claims 128-130 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji et al. (4,855,807) in view of Nokita (JP-2000-124396), Casto (5,014,113) and further in view of Huang (2002/0113305).

With regard to claims 128,129, Yamaji et al., Nokita and Casto do not disclose the die pad comprises divided first and second die pads wherein the first and second die pads each include a chip attaching part and peripheral part.

However, Huang discloses the die pad comprises divided first and second die pads (410,440) wherein the first and second die pads (410,440) each include a chip attaching part and peripheral part. (Note fig. 1 of Huang).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Yamaji et al., Nokita and Casto's device having the die pad comprises divided first and second die pads wherein the first and second die pads each include a chip attaching part and peripheral part such as taught by Huang in order to provide more space for accommodating semiconductor chips.

With regard to claim 130, Yamaji et al., Nokita and Casto do not disclose an adhesive bonds the semiconductor chip to the die pad chip attaching part, and an adhesive is attached to the backside of the chip in a wafer state to bond the semiconductor chips to the chip attaching part.

However, Huang discloses an adhesive 11a bonds the semiconductor chip to the die pad chip attaching part. An adhesive 11b is attached to the backside of the chip in a wafer state to bond the semiconductor chips (12a,12b) to the chip attaching part. (Note fig. 6 of Huang).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Yamaji et al., Nokita and Casto's device having an adhesive bonds the semiconductor chip to the die pad chip attaching part, and an adhesive is attached to the backside of the chip in a wafer state to bond the semiconductor chips to the chip attaching part such as taught by Huang in order to secure the interface between semiconductor chips and the die pads.

Claim 131 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji et al. (4,855,807) in view of Nokita (JP-2000-124396), Casto (5,014,113), Huang (2002/0113305) and further in view of Kozono (6,177,718).

Yamaji et al., Nokita, Huang and Casto do not disclose the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires.

However, Kozono discloses the lead frame 13 is made of iron-nickel alloy or copper alloy, and wherein the bonding wires 14 are gold wires. (Note lines 16-20, column 6, fig. 21 of Kozono).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Yamaji et al., Nokita, Huang and Casto's device having the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires such as taught by Kozono in order to prevent the lead frame from broken.

Allowable Subject Matter

3. Claims 22,118,137-142 allowable over the prior art of record, because none of these references disclose or can be combined to yield the claimed invention such as the peripheral part protruding towards only one of the first and second semiconductor chips as recited in claim 22, the peripheral part only protrudes downward as recited in claim 137, the peripheral part only protruding away from the semiconductor chip as recited in claim 142.

4. Claims 125 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 125 is allowable over the prior art of record, because none of these references disclose or can be combined to yield the claimed invention such as the tie bar has the same thickness as the leads as recited in claim 125.

Election/Restrictions

5. This application contains claims 30-49 drawn to an invention nonelected. A complete reply to the final rejection must include cancelation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Response to Arguments

6. Applicant's arguments filed 04/08/04 have been fully considered but they are not persuasive.

It is argued, at page 19 of the remarks, that "As was previously suggested by the examiner and as stated in claim 55, Casto's inner leads (those encapsulated by the encapsulant) do not totally have a constant second thickness that is greater than the first thickness). However, the previous amended suggestion of claim 55 is reconsidered by examiner, claim 55 still meet Casto's reference based on old prior art. Thus, Examiner made a new non-final rejection and claim 55 is moot in view of the new ground(s) of rejection as recited in the Response to Amendment of the last office action. Moreover, fig.1 of Casto does show the chip attaching part

having a first thickness and the inner leads 28 totally having a constant second thickness greater than the first thickness.

It is argued, at page 19 of the remark, that "claim 56 recites that the inner leads are formed of a single layer. To the contrary, Casto teaches a multiple-layer lead frame 16 (Fig. 1; column 3, lines 33-35; emphasis added) having a first frame layer 18 (Fig. 1; column 3, lines 34-35) and at least a second frame layer 28 bonded to the first frame layer 18 (Fig. 1; column 3, lines 40-41). Thus, Casto fails to anticipate claim 56". However, figs.1, 2 of Casto et al. does show the inner leads of the leads 28 are formed of a single layer.

It is argued, at page 20 of the remark, that "the peripheral part protrudes toward the second semiconductor chip and away from the first semiconductor chip (emphasis added). This amendment is fully supported by the application as filed at, e.g., FIG. 10. The Casto/Nokita combination fails to teach this feature". However, Note see attachment #1 of Nokita does show the peripheral part 1B protrudes toward the second semiconductor chip 5B and away from the first semiconductor chip 5B.

It is argued, at pages 21,22 of the remark, that "Neither Casto nor Nokita teach or suggest a peripheral part that protrudes toward a first semiconductor chip and away from a second semiconductor chip". However, Note see attachment #1 of Nokita does show the peripheral part 1A protruding towards the first semiconductor chip 5A and away from the second semiconductor chip 5B. Thus, Applicant's claims 20,21,23-29,50,51,55-71,73-80,82-116,118,120-124,126 and 128-136 do not distinguish over Casto, Kouda, Huang, and Nokita references.

7. Applicant's arguments with respect to claims 50,51,118,120-124,126,128-132 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Tan Tran whose telephone number is (571) 272-1923. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

TT

May 2004

Minhloan Tran
Primary Examiner
Art Unit 2826

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	21/60	３０１		23/50	Ｕ	

審査請求　未請求　請求項の数３　ＦＤ　（全　３　頁）　最終頁に続く

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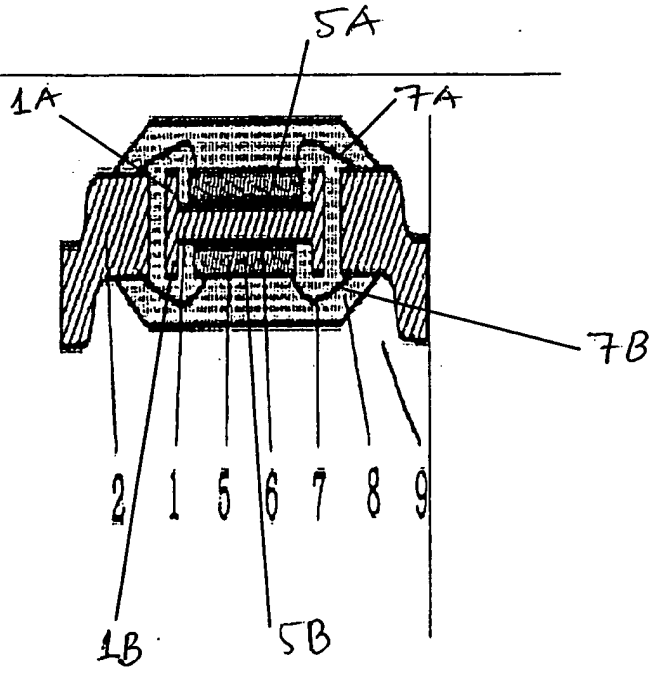
5F044 AA01 CC07 JJ03
5F047 AA11 AB03
5F067 AA01 AA02 AB03 BE02 CB00
DF01

(54)【発明の名称】　半導体装置

(57)【要約】
【課題】 半導体チップを両面に搭載し高集積、多機能性を備えさせることが出来ながら且つ薄手化でき、また耐損傷性、実装性もよい半導体装置を得る。
【解決手段】 両面側から厚みを薄くしたパッド１に、半導体チップ５が前記薄くした箇所に入り込んで搭載され、該半導体チップ５と前記パッド１の周りに設けたリード２とを金属線７で接続し、前記金属線７の接続箇所を含むリード部、パッド１、半導体チップ５を樹脂封止８して半導体装置を構成している。また、前記パッド１の厚みを薄くした深さは半導体チップ５の同等あるいはそれ以上にされ、樹脂封止８部から出ているリード２の下面は樹脂封止下面と同等あるいは若干下側に位置している。



Attachment # 1